REMARKS

Claims 1-20 are currently active.

The Examiner has rejected Claims 1-5 and 7 as being anticipated by Gritton. Applicants respectfully traverse this rejection.

The Examiner has rejected Claims 5-8 under 35 U.S.C. 112, second paragraph. Claims 5 and 7 have been amended to obviate this rejection.

On page 3 of the Office Action, the Examiner cites column 7, lines 30-40 of Gritton as support for teaching the limitation of "the memory comprising at least one linear time indexed array having a plurality of locations for buffering". Applicants respectfully submit the term linear time-index array is not taught or suggestion by Gritton.

Referring to column 7, lines 30-50, Gritton teaches a memory 46 is coupled to the segmenter 42 and scheduler 44 and is configured to store a plurality of linked cells as received from segmenter 42 in defined slots. Also, memory 46 is configured to store scheduling lists and data as received from scheduler 44. In other embodiments, either segmenter 42 and/or memory 46 can function to manage the slots defined within memory 46.

By way of example, segmenter 42 may be required to locate the address location of the next available slot within memory 46. Similarly, one scheduler 44 has transmitted the cell within a slot, or otherwise empty this slot, but it may be required to communicate to either segmenter 42 and/or memory 46 that the slot is now available for re-use. As is apparent from the above description, there is no teaching or suggestion whatsoever of a linear time-indexed array taught or suggested by Gritton. For a claim to be anticipated by a reference, the limitation must be specifically found in the four corners of the document. This is not the case in regard to this limitation in Gritton. Accordingly, it is respectfully submitted that Claims 1-5 and 7 are not anticipated by Gritton.

The Examiner has rejected Claims 1-20 as being anticipated by Chao. Applicants respectfully traverse this rejection.

The Examiner cites column 18, lines 15 and 16; and column 16, line 16 as support for the limitation of "the memory comprising at least one linear time-index array having a plurality of locations for buffering the at least one data unit". The Examiner in regard to the limitation of Claim 1 "in the event the at least one data unit is associated with a plurality of channels in the network, dividing the memory into a plurality of linear time-indexed arrays, each time-indexed array corresponding to a respective channel, and storing the at least one data unit in a respective location of the corresponding time-indexed

array", simply states that regardless of the number of channels, such that if there is one channel or a plurality of channels, they will perform the functions. See page 5 of the Office Action.

Referring to column 18, lines 15 and 16, Chao states in each of the columns, packets are sorted according to their time stamps. Column 16, line 16 states the article "Switched Prioritized Packets" discusses a searching method where a number of timing queues are maintained for distinct time stamp value. As is apparent, and as the Examiner recognizes, Chao is only applicable to a single queue. The Examiner's further comment that a plurality of channels will perform the same function, ignores the specific limitation in Claim 1 of "in the event the at least one data unit is associated with a plurality of channels in the network, dividing the memory into a plurality of linear time-indexed arrays". This limitation is distinct and not taught or suggested by Chao and is different then just having a plurality of time-indexed arrays, each associated with a channel.

Applicants' claimed invention is more distinct with the limitation that there has to be a data unit that is associated with a plurality channels, and then the memory is divided into a plurality of time-indexed arrays. There is no teaching or suggestion in Chao of the triggering event being the one data unit is associated with a plurality of channels, and the dividing the memory into a plurality of linear time-indexed arrays. While Chao teaches a

single time-indexed array, and the Examiner suggests that a plurality of time-indexed arrays serves the same function, there is no teaching or suggestion of only forming the plurality of time-indexed arrays from the memory when the single data unit is associated with a plurality of channels and will appear in the network. Thus, it is respectfully submitted there is much more in regard to the limitation just discussed of Claim 1 and simply a plurality of time-indexed arrays. For these reasons, Claim 1 is not anticipated by Chao. Claims 2-20 are patentable for the reasons Claim 1 is patentable over Chao.

The Examiner has rejected Claims 6 and 8 as being unpatentable over Gritton in view of Chao. Applicants respectfully traverse this rejection. Claims 6 and 8 are dependent on Claim 1 and are patentable for the reasons Claim 1 is patentable. As explained above in regard to both Chao and Gritton, Claim 1 is patentable over each one separately, and combining the teachings still fails to arrive at the limitations of Claim 1 discussed above. Accordingly, Claims 6 and 8 are patentable over Gritton in view of the Chao.

In view of the foregoing amendments and remarks, it is respectfully requested that the outstanding rejections and objections to this application be reconsidered and withdrawn, and Claims 1-20, now in this application be allowed.

Respectfully submitted,

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